IN THE SPECIFICATION:

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Please amend paragraph number [0007] as follows:

[0007] FIGS. 27-31 illustrate a common method of forming a cobalt silicide layer on an active-device region of a thin film semiconductor device. FIG. 27 illustrates an intermediate structure 400 comprising a semiconductor substrate 402 with a polysilicon layer 404 thereon, wherein the polysilicon layer 404 has at least one active-device region 406 formed therein with a thin dielectric layer 408, such as tetraethyl orthosilicate - TEOS, disposed thereover. The thin dielectric layer 408 must be as thin as possible to reduce the height of the thin film semiconductor device. A contact opening 412 is formed, by any known technique, such as patterning and etching, in the thin dielectric layer 408 to expose a portion of the active-device region 406, as shown in FIG. 28. A thin layer of cobalt 414 is applied over the thin dielectric layer 408 and the exposed portion of the active-device region 406, as shown in FIG. 29. A high temperature anneal step is conducted in an inert atmosphere to react the thin cobalt layer 414 with the active-device region 406 in contact therewith which forms a cobalt silicide layer 416, as shown in FIG. 30. However, dielectric materials, such as TEOS - tetraethyl orthosilicate, BPSG - borophosphosilicate glass, PSG - phosphosilicate glass, and BSG - borosilicate glass, and the like, are generally porous. Thus, the thin dielectric layer 408 has imperfections or voids which form passages through the thin dielectric layer 408. Therefore, when the high-temperature anneal is conducted, cobalt silicide also forms in these passages. The cobalt silicide structures in the passages are referred to as patches 418, as also shown in FIG. 30. When the nonreacted cobalt layer 414 is removed to result in a final structure 422 with a cobalt silicide layer 416 formed therein, as shown in FIG. 31, the patches 418 also form conductive paths between the upper surface of the thin dielectric layer 408 which can cause shorting and current leakage on IC backend testing devices which leads to poor repeatability and, thus, poor reliability of the data from the testing devices.

Please amend paragraph number **[0026]** as follows:

[0026] FIG. 1 illustrates a semiconductor substrate 100, such as a silicon-containing substrate, having a polysilicon layer 102 thereon, wherein at least one active-device region 104 is formed in a polysilicon layer 102, with a thin dielectric layer 106, such as TEOS, of a thickness of approximately 1 kÅ disposed over the polysilicon layer 102. A layer of barrier material layer 108, preferably titanium nitride deposited to a thickness of between about 100-150Å, is deposited over the thin dielectric layer 106, such as by PVD, as shown in FIG. 2. Other potential barrier materials include tungsten nitride, tungsten silicon nitride, titanium silicon nitride, and the like.

Please amend paragraph number **[0040]** as follows:

[0040] The nonreacted cobalt layer 318 is removed, preferably by a wet etch, such as hydrochloric acid/peroxide or sulfuric acid/peroxide mixtures, wherein the barrier material layer 314 preferably acts as an etch stop, as shown in FIG. 25. As shown in FIG. 26, the remaining barrier material layer 314 and the remaining polysilicon layer 308 are removed.